WHAT IS CLAIMED IS:

1. A semiconductor device that accesses at least one semiconductor storage medium, comprising:

a bus master;

a bus interface that controls access to the at least one semiconductor storage medium based on request for access to the at least one semiconductor storage medium from the bus master; and

a clock-supply-control circuit that controls the presence of the supply of a clock to the bus interface based on access state information that indicates a state of access to the at least one semiconductor storage medium, the clock-supply-control circuit including a circuit, the circuit implementing at least one of control for stopping the supply of the clock to the bus interface if the circuit determines that access is not in execution, and control for supplying the clock to the bus interface if the circuit determines that access is in execution, based on the access state information.

2. The semiconductor device according to Claim 1,

the at least one semiconductor storage medium including at least a plurality of semiconductor storage media;

the bus interface including:

a common bus interface that in common implements operation required for access control when access to any of the semiconductor storage media is in execution; and

dedicated bus interfaces that each correspond to a certain one of the semiconductor storage media and that each implement operation required for access control only when access to the certain one of the semiconductor storage media is in execution; and

the clock-supply-control circuit detects any of the semiconductor storage media that is other than any of the semiconductor storage media that is to be accessed based on accessed-medium information indicating which semiconductor storage medium is to be accessed, and controls so as to stop the supply of the clock to any of the dedicated bus interfaces for the any of the semiconductor storage media that is other than the any of the semiconductor storage media that is to be accessed and supply the clock to any of the dedicated bus interfaces for the any of the semiconductor storage media that is to be accessed.

3. The semiconductor device according to Claim 1, the clock-supply-control circuit implementing a processing to stop the supply of the clock to the bus interface after the completion of a valid signal output from the bus interface.

4. A semiconductor circuit that controls a presence of a supply of a clock to a bus interface controlling access to at least one semiconductor storage medium based on request for access to the at least one semiconductor storage medium from a bus master, comprising:

a control-signal generator that generates a clock-supply-control signal for the bus interface for instructing the presence of the supply of the clock to the given bus interface, based on access state information that indicates a state of access to the at least one semiconductor storage medium; and

a control circuit that controls the presence of the supply of the clock generated from a clock generator to the given bus interface, based on the clock-supply-control signal for bus interface,

the control-signal generator disabling the clock-supply-control signal for bus interface if the access state information indicates that access is not in execution; and

the control circuit including a circuit that controls so as to stop the supply of the clock generated from the clock generator to the bus interface if the clock-supply-control signal for bus interface is disabled.

5. The semiconductor circuit according to Claim 4,

the at least one semiconductor storage medium includes at least a plurality of semiconductor storage media;

the bus interface includes:

a common bus interface that in common implements operation required for access control when access to any of the semiconductor storage media is in execution; and

dedicated bus interfaces that each correspond to a certain one of the semiconductor storage media and that each implement operation required for access control only when access to the certain one of the semiconductor storage media is in execution; and

the control-signal generator detects any of the semiconductor storage media that is other than any of the semiconductor storage media that is to be accessed based on accessed-medium information shown by the bus interface and indicating which semiconductor storage medium is to be accessed, so as to disable a clock-supply-control signal for dedicated bus interface to any of the dedicated bus interfaces for the any of the semiconductor storage media that is other than the any of the semiconductor storage media that is to be accessed; and

the control circuit includes a circuit that controls so as to stop the supply of the clock generated from the clock generator to the any of the dedicated bus interfaces for the any

of the semiconductor storage media that is other than the any of the semiconductor storage media that is to be accessed if the clock-supply-control signal for dedicated bus interface is disabled.

6. The semiconductor circuit according to Claim 4, the control-signal generator disabling the clock-supply-control signal for dedicated bus interface after the completion of a valid signal from the bus interface.

7. Electronic equipment, comprising:

a semiconductor device that includes the semiconductor device according to Claim 1;

an input device that receives input information; and

an output device that outputs a result processed by an information-processing device based on the input information.

8. Electronic equipment, comprising:

a semiconductor device that includes the semiconductor circuit according to Claim 4;

an input device that receives input information; and

an output device that outputs a result processed by an information-processing device based on the input information.

9. A method of controlling clock-supply that controls the presence of a supply of a clock to a bus interface of a semiconductor device, comprising:

generating a clock-supply-control signal for the bus interface for instructing the presence of the supply of the clock to a given bus interface, based on access state information that indicates a state of access to at least one semiconductor storage medium; and

controlling the presence of the supply of the clock generated from a clock generator to the given bus interface, based on the clock-supply-control signal for bus interface,

the clock-supply-control signal for bus interface being disabled if the access state information indicates that access is not in execution; and

control to stop the supply of the clock generated from the clock generator to the bus interface block being implemented if the clock-supply-control signal for bus interface is disabled.

10. The method of controlling clock-supply according to Claim 9,

the at least one semiconductor storage medium including at least a plurality of semiconductor storage media;

the bus interface including:

a common bus interface that in common implements operation required for access control when access to any of the semiconductor storage media is in execution; and

dedicated bus interfaces that each correspond to a certain one of the semiconductor storage media and that each implement operation required for access control only when access to a certain one of the semiconductor storage media is in execution;

any of the semiconductor storage media that is other than any of the semiconductor storage media that is to be accessed is detected based on accessed-medium information shown by the bus interface and indicating which semiconductor storage medium is to be accessed, and a clock-supply-control signal for dedicated bus interface to any of the dedicated bus interfaces for the any of the semiconductor storage media that is other than the any of the semiconductor storage media that is to be accessed is disabled; and

control is implemented so that the supply of the clock generated from the clock generator to the any of the dedicated bus interfaces for the any of the semiconductor storage media that is other than the any of the semiconductor storage media that is to be accessed is stopped if the clock-supply-control signal for dedicated bus interface is disabled.

11. The method of controlling clock-supply according to Claim 9, the clock-supply-control signal for the dedicated bus interface being disabled after the completion of a valid signal from the bus interface.